UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/628,059	07/28/2000	Fan Zhou	FORE-71	2638

7590 11/19/2004	EXAMINER
Ansel M Schwartz	KADING, JOSHUA A

ART UNIT	PAPER NUMBER
2661	

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DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/628,059	ZHOU ET AL.
	Examiner	Art Unit
	Joshua Kading	2661

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _30 September 2004_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
    closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-21_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _13-21_ is/are allowed.

6)☒ Claim(s) _1-3_ is/are rejected.

7)☒ Claim(s) _4-12_ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some *   c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
        application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can

be found in a prior Office action.

5   Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Chiussi et al. (U.S. Patent 5,689,506) in view of Parruck et al. (U.S. Patent 6,229,812

B1) in further view of Newman (U.S. Patent 5,367,518) and further in view of Yamanaka

et al. (U.S. Patent 5,619,495).

10   In regard to claim 1, Chiussi discloses "a switch for switching packets in a

network comprising:

a plurality of port cards which send packets to and receive packets from the

network" (figure 11, elements 1110 and 1150); and

"a parity stripe from which the packets are reconstructed with the parity stripe

15   providing for error detection and correction (figure 5, where the HCC stripe is meant to

be the HEC or Header Error Control as read in col. 6, lines 14-23 and as seen in figure

5 the "old" packet and the "new" packet both contain the HEC parity stripe)...each fabric

having a plurality of queues in which portions of packets...are stored, each queue

corresponding to one of the port cards..." (figure 11, where element 1130 constitutes a

20   fabric used for switching portions of the packets; figures 3, and 4 where the input ports

have a plurality of queues in them as is read in col. 3, lines 65 where the buffering is

taken to mean there are buffers or queues in the ports; and as can be seen from figures

3, 4, and 11 the inputs to the fabric corresponds to one input per port card).

However, Chiussi lacks what Newman discloses, that is "a plurality of fabrics

connected to the port cards for switching portions of the packets (figure 13, elements 8-

5   0, 8-1 where each fabric of the plurality of fabrics operates according to the fabric of

Chiussi et al.).

It would have been obvious to one with ordinary skill in the art at the time of

invention to include the plurality of switching fabrics in place of the single fabric for the

purpose of increasing switching throughput. The motivation being to allow for a higher

10   data switching rate.

Chiussi and Newman also lack what Parruck discloses, that is "...each fabric

having a determining mechanism which determines which queue the portions of the

packet should be placed in, the determining mechanism is dynamic to reflect changes in

the port card quantity without any change in connection data of the packets (figure 3,

15   where it is clear that the data coming in on element 310 is routed or sent by a

mechanism to the appropriate queue elements 302(a-x); it should also be noted that if

the port card quantity were to change the determining mechanism would still be able to

send the data to the appropriate queue and to thus to the final destination, allowing the

connection data to remain intact)."

20   It would have been obvious to one with ordinary skill in the art at the time of

invention to include the "determining mechanism" with the switching mechanism to

further assist the routing capabilities of the switch. The motivation being to allow for

faster switching by "presorting" the data with the determining mechanism.

Chiussi, Newman, and Parruck also lack what Yamanaka discloses, that is the

packets are portions of packets, or "stripes" (figure 30 where the header processing unit

5   separates the header from the data effectively turning them into fragments, or stripes).

It would have been obvious to one with ordinary skill in the art at the time of

invention to include the "stripes" with the rest of the switch for the purpose of processing

regular data and address data simultaneously. The motivation being that the dual

processing allows for a faster switching process.

10

In regard to claim 2, Chiussi, Parruck, Newman, and Yamanaka disclose the

switch according to claim 1. Chiussi, Newman, and Yamanaka lack "each fabric has a

memory controller having the queues and the determining mechanism." However,

Parruck further discloses "each fabric has a memory controller having the queues and

15   the determining mechanism" (figure 3 where the determining mechanism as defined in

claim 1 and the queues, elements 302(a-x), can be considered part of the same

component; in this case the memory controller has the queues (memory) and the

determining mechanism (controller) all in one component as can be seen in figure 3). It

would have been obvious to one with ordinary skill in the art at the time of invention to

20   put the "determining mechanism" with the "queues" in a "memory controller" for the

reasons and motivation as in claim 1.

In regard to claim 3, Chiussi, Parruck, Newman, and Yamanaka disclose the

switch according to claim 2. Parruck, Newman, and Yamanaka lack "...an input lookup

which identifies in which queue portions of the packet are placed." However, Chiussi

further discloses "...an input lookup which identifies in which queue portions of the

5   packet are placed" (figure 8, where the tables represent address tables that store the

addresses of the incoming data, thus storing the location of the data in the queues). It

would have been obvious to one with ordinary skill in the art at the time of invention to

include the "input lookup" with the "determining mechanism" of claim 2 for the purpose

of having a list of the location of the data. The motivation being to allow for easy access

10   to the data by use of the lookup.

Allowable Subject Matter

Claims 4-12 are objected to as being dependent upon a rejected base claim, but

would be allowable if rewritten in independent form including all of the limitations of the

15   base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject

matter: Claims 13-21 are allowable because the prior art of record fails to teach, in

combination with other claim limitations, "changing the number of port cards in the

20   switch".

Response to Arguments

Applicant's arguments filed 30 September 2004 have been fully considered but they are not persuasive. Applicant states that neither Chiussi, Parruck, Newman, nor Yamanaka disclose "portions of packets as stripes and a parity stripe from which the packets are reconstructed with the parity stripe providing for error detection and

5   correction". The examiner respectfully disagrees.

Regarding the error detection and correction parity stripe, Chiussi fully discloses the use of error correction data in the header or each packet old and new (wherein new being translated) by way of the HEC portion of the packet. Further, Yamanaka discloses that the portions of packets are stripes, i.e. fragments. If applicant does not intend the

10   term "stripes" to mean fragments, then the term must be defined in the applicant's specification. See MPEP § 2106.II(c).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua Kading whose telephone number is (571) 272-

15   3070. The examiner can normally be reached on M-F: 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

5   For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Joshua Kading
Examiner
Art Unit 2661

10   November 9, 2004

BOB PHUNKULH
PRIMARY EXAMINER